and so the ratio

$$\frac{I_d}{g_m} = \frac{1}{n}(V_p + V_g) \qquad (3)$$

should give a straight line when plotted on linear scales as a function of V_g. Further, the pinch-off voltage and the exponent are obtained directly as the intercept on the voltage axis and the reciprocal slope of the straight line.

Plots of (3) for p-n junction FET's of various structures are shown in Fig. 1, and the resulting values of V_p and n are given in Table I. It is seen that the experimental points do indeed define straight lines quite closely, thus vindicating the postulated power-law relation of (1). Moreover, the values of n obtained are reasonably close to 2, thus lending weight to the simple theoretical square-law derivation of the accompanying communication. The departure from a straight line in some units near the pinch-off voltage is due to drain leakage current, and is the effect that prevents direct measurement of the pinch-off voltage. The maximum in I_d/g_m that occurs at small positive gate voltages is to be expected on theoretical grounds, and is not significant in determining the best-fit straight line over the range $0 < |V_g| < V_p$.

It is concluded that the power-law relation of (1) satisfactorily represents both theoretically and experimentally the transfer characteristics of an FET in the pinch-off region, and allows values of the pinch-off voltage and the exponent to be determined directly from experimental measurements.

A future communication will show theoretically why the values for the exponent n obtained experimentally are so close to the value 2 derived by the approximate treatment in the accompanying communication.

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I. Richer
R. D. Middlebrook
Div. Eng. and App. Sci.
California Institute of Technology
Pasadena, Calif.

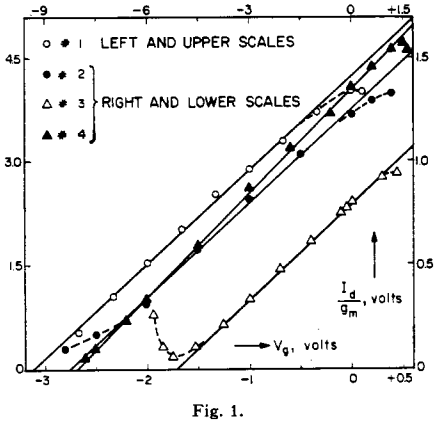

Fig. 1.

TABLE I

Measurement Conditions: Frequency = 1 kc
$|V_d| = 25$ v (#1), $|V_d| = 10$ v (#2–#4)

Unit	Type	Nature of junction	V_p volts	n
#1	Crystalonics 610	alloy (n-channel)	9.33	2.20
#2	Motorola MM 764	epitaxial (n-channel)	2.74	2.18
#3	Texas Instruments TIX 691	diffused (p-channel)	1.70	2.15
#4	Fairchild FSP 401	diffused (n-channel)	2.68	1.98

A Simple Derivation of Field-Effect Transistor Characteristics*

In the conventional treatment of the field-effect transistor, the first step is the specification of an impurity profile that describes the nature of the gate-channel contact. Solutions for the static and small-signal characteristics are then valid only for the particular impurity profile chosen, and must be repeated from the beginning for different structures.

The purpose of this communication is to present a simple, though approximate, development of the characteristics of an FET without specifying the detailed nature of the structure. The charge-control approach is used,[1,2] and it is shown that in the pinch-off region the relation between the drain current and the gate-source voltage is approximately square law. The results are applicable to all gate-channel structures, including the insulated gate types.

The basic model of an n channel FET (field-effect transistor) is shown in Fig. 1. One-dimensional current flow in the channel of length L is assumed to occur under the influence of a drain-source voltage V_d and a gate-source voltage V_g. The method of solution is to calculate the drain current I_d from the fundamental charge-control relation $I_d = Q/\tau_t$ where τ_t is the average transit time of the mobile carriers making up the total charge Q in transit between source and drain. The total mobile charge Q in the channel can be considered as made up of two parts: one part, Q_c, is the charge which would exist in the absence of the gate structure; the other part, Q_g, is the additional charge induced by a gate voltage.

The basic simplifying assumption to be made is that the potential drop in the channel is uniform so that the electric field is constant and equal to V_d/L. If the mobile carriers have constant mobility μ, the drift velocity is constant at $\mu V_d/L$ and the transit time is $\tau_t = L^2/\mu V_d$. The drain current is $I_d = (Q_c + Q_g)/\tau_t = G_c(1 + Q_g/Q_c)V_d$ where $G_c \equiv \mu Q_c/L^2$ is identified as the channel conductance in the absence of the gate structure, and in which the additional charge Q_g may be expressed as a function of the average voltage between gate and channel. Under the assumption of constant channel field, this average voltage is $(V_g - V_d/2)$ and the additional channel charge may be written $Q_g = C_g(V_g - V_d/2)$ where C_g represents a capacitance which, under certain conditions, may be identified as the total gate capacitance. Hence the drain current is given by

$$I_d = G_c\left(1 + \frac{V_g - V_d/2}{Q_c/C_g}\right)V_d. \qquad (1)$$

The above equation describes approximately the drain characteristics of the device in the region where the incremental drain conductance $\partial I_d/\partial V_d$ is finite, as indicated in Fig. 2. From the above equation, the drain conductance is

$$\frac{\partial I_d}{\partial V_d} = G_c\left(1 + \frac{V_g - V_d}{Q_c/C_g}\right) \qquad (2)$$

which goes to zero when $V_d - V_g = Q_c/C_g$. The drain current for which the drain conductance is zero is therefore given as a function of gate voltage by substitution of this condition on V_d back into (1), which leads to

$$I_d = \frac{G_c}{2}\frac{Q_c}{C_g}\left(1 + \frac{V_g}{Q_c/C_g}\right)^2 \qquad (3)$$

If the gate voltage is chosen so that $V_g = -Q_c/C_g$, the drain current is zero and

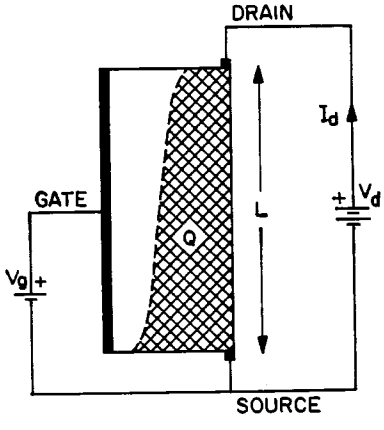

Fig. 1.

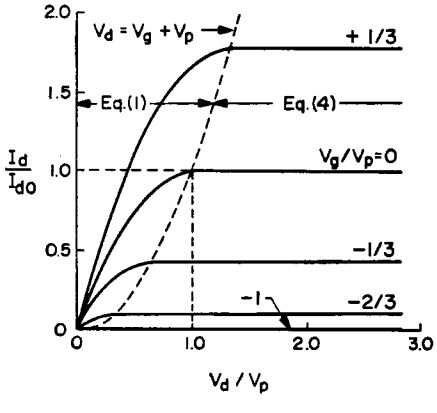

Fig. 2.

* Received May 13, 1963. The work reported here was supported in part by funds made available by the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, under NASA Contract No. NAS 7-100.

[1] E. O. Johnson and A. Rose, "A simple general analysis of amplifier devices with emitter, control, and collector functions," Proc. IRE, vol. 47, pp. 407–418; March, 1959.

[2] R. D. Middlebrook, "A modern approach to semiconductor and vacuum device theory," *Proc. IEE*, vol. 106, pt. B, suppl. no. 17; pp. 887–902; May, 1959.

hence $V_p \equiv Q_c/C_g$ is identified as the pinch-off voltage. To a first approximation, therefore, the drain conductance is zero when the drain voltage equals or exceeds $V_p + V_g$. In normalized form, (3) may be written

$$I_d = I_{d0}(1 + V_g/V_p)^2 \qquad (4)$$

where I_{d0} is the drain current in the pinch-off region when $V_g = 0$. Eq. (4) thus describes approximately the drain characteristics beyond pinch-off, as indicated in Fig. 2.

The transconductance g_m in the pinch-off region is obtained from (3) as $g_m \equiv dI_d/dV_g = G_c(1 + V_g C_g/Q_c)$, which shows the well-known result that the transconductance at zero-gate voltage is equal to the total channel conductance in the absence of the gate structure.

The square-law dependence of drain current upon gate voltage is only approximate, not only because of the initial assumption of constant channel field, but also because the capacitance C_g in general is not constant, but is a function of both V_g and V_d. However, when the drain voltage equals or exceeds the pinch-off voltage, C_g is essentially independent of V_d and hence the result of (2) is valid when used to obtain the characteristics beyond pinch-off. Nevertheless, the parameters I_{d0} and V_p in (4) in general remain dependent, though only weakly so, upon V_g.

The simple square-law functional relation of (4) has been derived without specification of the channel impurity profile or of the nature of the gate contact, and is valid for negative V_g/V_p (p-n junction FET's) and for either positive or negative V_g/V_p (insulated-gate FET's). Experimental substantiation of this power law is presented in an accompanying communication.[3]

R. D. Middlebrook
Div. Eng. and App. Sci.
California Institute of Technology
Pasadena, Calif.

[3] I. Richer and R. D. Middlebrook, "Power-law nature of field-effect transistor experimental characteristics," this issue, pp. 1145–1146.

Nanovolt Transistor dc Amplifiers*

The major limitation in the design of low-level transistor dc amplifiers has always been considered to be the drift resulting from the variations in parameters of transistors with temperature. In the differential configuration, the null stability has been mainly limited by the unavoidable mismatch in the thermal coefficients of the transistor parameters. A considerable improvement has been achieved by the use of a compensation circuit.[1] However, the degree of compensation is again limited by the temperature differential between the transistors and the compensation network.

We have developed a new type of differential configuration, in which the compensation is realized by the transistors themselves.[2] For this reason, this configuration may be referred to as "self-compensating." The drift can be cancelled to such a degree that the low-level limitation in transistor dc amplifiers seems now to be the low-frequency noise.

For reasonably small source resistances and low operating collector currents, the dominant component of the thermal drift in silicon transistors normally arises from the mismatch in the temperature coefficients of the base-emitter voltages. This temperature coefficient of V_{BE} is predictable on well-established theoretical grounds, and, to a high degree of accuracy, it depends only on V_{BE} itself. Thus it appears that the match of the temperature coefficients of V_{BE} should be improved by operating the two transistors with equal base-emitter voltages, rather than with the conventional procedure of using equal collector currents and matched collector resistances.

These conditions of operation with matched V_{BE} can be realized in a floating input stage as shown in Fig. 1 where R_c is made equal to zero and R_d is adjusted in order to have the same base voltages. The need for R_c and the network containing R_b will appear later. The zero adjustment (*i.e.*, the condition zero output for zero input signal) is realized by unbalancing the collector load resistors by means of potentiometer R_a.

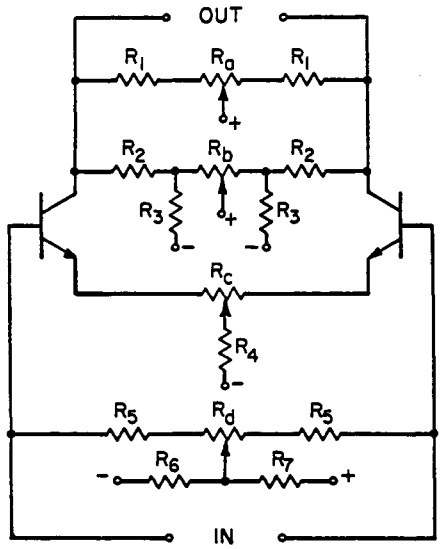

Fig. 1—A self-compensating dc amplifier.

The use of a floating input stage is convenient since the common-mode rejection factor is greatly affected by circuit unbalances. Furthermore, with a floating stage, the common-mode signal will not affect the operating conditions of the transistors. The common-mode rejection problem can be taken care of in the following stages.

In this simple configuration and under the conditions of operation described above, it turns out, both in theory and in fact, that the null stability is very little affected by power supply variations and by the common-mode variations of V_{BE}. The thermal drift is not completely cancelled, however, because the temperature coefficients of V_{BE} are still slightly unbalanced and the other components of the thermal drift may be significant. At any rate, the thermal drift is reduced typically by a factor of 5 in comparison with the drift occuring in the conventional equal-current operation.

Further compensation can be achieved by taking advantage of the fact that the temperature coefficient of V_{BE} depends on V_{BE}. Thus, by operating the two transistors at slightly different base-emitter voltages, it is possible to equalize their temperature coefficients, and even better, it is possible to cancel the over-all thermal drift due to all components.

These conditions of operation can be realized by unbalancing potentiometer R_c. Again, R_d is adjusted to equalize the base voltages and R_a is adjusted for zero output.

However, with such a procedure, the effects of power supply variations may become significant. Power supply compensation can be achieved by further unbalancing the collector resistances and correcting the zero offset with R_b. It should be noted that there are interactions between the different effects so that much care must be taken to determine the compensating elements.

Thus, with the four potentiometers R_a, R_b, R_c and R_d, the circuit possesses four degrees of freedom. It is possible, by a systematic procedure, to satisfy the four following conditions:

1) Zero output for zero input voltage.
2) Zero output for zero input current.
3) Compensation for temperature variations.
4) Compensation for power supply variations.

In the realization of this circuit, we have used matched high gain ($\beta > 200$) transistors constructed on the same header (dual matched 2N2484's supplied by Fairchild Semiconductor), metal film resistors and wire wound potentiometers, and a mercury cell as a power supply. The compensation conditions could be achieved with relatively slight unbalances in the circuit.

A thermal drift of less than 0.05 μv/°C referred to the input has been achieved. Power supply variation of 1 per cent has led to an equivalent input drift less than 0.2 μv. Over-all drift less than 0.4 μv over extended periods of time has been observed.

It appears then that the low-frequency fluctuations which were of the order of 0.5 μv peak to peak will dictate the low-level limitations in transistor dc amplifiers.

Further studies of the low-frequency noise and its bias dependence are in progress. There appears to be reasonable hope for reducing long-term drift and noise to the order of 200 nanovolts while maintaining bandwidths greater than 10 kc/sec. A more detailed discussion and experimental results will be presented in a future paper.

A. H. Hoffait
R. D. Thornton
Dept. of Elec. Engrg.
Mass. Inst. Tech.
Cambridge, Mass.

* Received May 20, 1963.

[1] R. D. Middlebrook and A. D. Taylor, "Differential amplifier with regulator achieves high stability, low drift," *Electronics*, vol. 34, pp. 56–59; July, 1961.

[2] We are familiar with similar work being done by D. Hilbiber of Fairchild Semiconductor, Palo Alto, Calif., and Prof. R. Black of the University of California, Berkeley.